Abstract

Due to the advancement of CMOS technology, diverse functions are getting integrated on an Integrated Circuit (IC) leading to high performance System on Chip (SOC) implementation At the same time the process sequence to build an IC is becoming very complex, demanding stringent process control to minimize the fluctuations in the transistor parameters The transistor parameter fluctuations due to the statistical nature of the underlying processes has a significant impact on the yield Yield refers to the percentage working chips, satisfying the performance constraints Computer simulation methodology using various Computer Aided Design (CAD) techniques and Technology CAD (TCAD) tools for assessing the performance and the yield of ICs is a key to the success of the IC manufacturing industry, in terms of cost, and time at various phases of manufacturing

We have used Integrated-System-Engineering (ISE) TCAD tool suite in characterizing transistor mismatch of 100nm CMOS devices We have first designed the best possible 100nm nominal NMOS/PMOS devices as per the specification of International Technology Roadmap for Semiconductor (ITRS) The disposable spacer process technique is used to obtain the optimized transistor structure DIOS-ISE process simulator is used to get the realistic transistor structure The physical effects such as doping and field dependence of mobility, velocity overshoot, channel carrier quantization, Band-To-Band-Tunneling (BTBT), have been considered for the device simulation

The impact of implant dose variation on the 100nm CMOS inverter performance is characterized using mixed-mode simulation The four implant steps namely, pocket halo, Super-Steep-Retrograde-Channel (SSRC), deep source/drain (s/d), and shallow extension are varied around their respective nominal values A 3σ variation of $\pm 10\%$ is assured around the nominal dose The Worst-Case-Analysis (WCA) approach is used to study the inverter delay fluctuation at the process

corners It is observed that the variation in inverter delay is highly nonlinear with respect to the process variation Further pocket halo and SSRC implants are found to have the greatest impact on the device/circuit parameter fluctuation A second order model has been derived using full factorial technique (3^4 experiments) to relate the device parameters such as threshold voltage, drain current to the implant dose variables This model enables us to obtain the statistical distribution of various device parameters

Then we have extended our study to characterize the 100nm CMOS devices in terms of all the constituent process steps that can result in variability We have used Design-of-Experiment (DOE) and Response-Surface-Modeling (RSM) techniques to handle the large input parameter space We have first identified 21 process parameters arising from different process steps If we use all 21 parameters for modeling through conventional full factorial 2^k (for first order modeling) or 3^k (for second order modeling) experimentation technique (k=21), the number becomes impractical to manage In order to get around this issue, we have done DOE and experimentation in 2 phases The first phase is the DOE based screening experiment using Plackett-Burman (PB) technique Here the first order model similar to the truncated Taylor's series for 21 variables has been fit to study the significance of individual input parameters The drive current, off state current, threshold voltage, and subthreshold slope in linear and saturation region are chosen to be the output (device) parameters of interest Four rounds of PB screening experiments, each with 28 runs, are conducted using ISE-TCAD tool While performing the screening experiments, the levels of all input process parameters except temperatures are varied by $\pm 10\%$ ($\pm 3\sigma$) around their nominal value The temperature variables are varied by $\pm 10^{o}$C around the nominal value We have selected 10 top ranking parameters to continue our RSM study In order to check the validity of ignoring 11 relatively insignificant variables, we have performed Monte-Carlo (MC) study to obtain the distribution of output parameters as a function of all 21 parameters as well as a function of the top 10 ranking parameters The results of MC process/device simulation study ensure the validity of the screening experiment

We have performed RSM of 8 key device parameters, based on the results of the screening experiment In order to generate the response surfaces, we have used a highly fractionated 3 level Face Centered Central Composite (FCCC) DOE This will cut down the number of process/device

simulations to 1045 compared to 3^{10}=59049 for the full factorial case Each of the resulting second order models, which are in the form of truncated Taylor's series for 10 variables have 66 terms The model is able to capture the 2^{nd} order cross interaction of the input variables The models are verified by performing MC simulations to compare the distributions generated by the model versus the distributions generated by the 10 significant parameters based process/device simulations We observe that the model is able to capture the trends in the process fairly well Using these models, response surfaces for output parameters can be generated to gain insight into the process control targets to realize certain objectives The Response-Surface-Analysis (RSA) is performed for each device parameters using their respective models to draw useful conclusions

Since the variability is increasing with the feature size reduction due to technology scaling, it becomes especially important to characterize the effect of new processes and new transistor structure on variability In this context we have compared the conventional dual poly gate CMOS devices with midgap metal gate (single gate for NMOS/PMOS) and bandedge metal gate (different gates for NMOS/PMOS) structures in chapter 6 This comparison is done from the perspective of high performance digital application as well as mixed-signal/analog applications When implant dose variations and the gate length variations are combined together, the midgap metal gate structure outperforms the other structures for high performance digital applications The midgap metal gate results in fastest inverter circuit and the delay variation is comparable to the poly gate The bandedge structure yields the lowest variability Typically the analog blocks are designed using larger gate length transistors to minimize variability Hence it is important to characterize analog metrics for larger lengths The midgap metal gate structure shows a stronger dependence of threshold voltage V_t on channel length This is expected since the work function difference contributes identically to short and long channel transistors Hence the transconductance at longer lengths will be lower for midgap metal gate However for $L_g > 0\ 25\mu$m the percentage variation in V_t for midgap metal gate is lower than the other structures Also the output resistance and intrinsic gain is the highest for the midgap metal gate structures